process expanded coefficient and word sizes. Multiple circuits can be cascaded for larger filter lengths at up to 20 MHz sample rate or a one or more DFP circuits can process larger filter lengths at less than 20 MHz. The architecture permits processing filter lengths up to 1028 taps with no overflows. The circuit supports unsigned or two's complement arithmetic, independently selectable for coefficients and signal data.

Each cell (MAC stage) contains three resampling or decimation registers which permit output sample rate reduction at rates of one-half, one-third, or one-fourth the input sample rate. These registers also provide the capability to perform 3×3 or 4×4 convolutions for image processing applications using one DFP. A 256×256×8 image can be convolved with a 3×3 kernel in real time (i.e., 6.64 MHz video rate).

Before describing the circuit structure and function, the following interface signal descriptions for the logic symbol of FIG. 1 are provided:

V_{cc} +5V power supply input (±5%)

V_{ss} Power supply ground input.

CLK The CLK input provides the DFP system sample clock. The clock must have a 50% duty cycle. The maximum clock frequency is 20 MHz for the ZR33481. The minimum frequency is 200 KHz.

DIN 0–7 These 8 inputs are the data sample input bus. Eight-bit data samples are synchronously input through these pins to the X REGISTER of each multiply-accumulate (MAC) cell of the DFP simultaneously. The $\overline{\text{DIENB}}$ signal enables loading, which is synchronous to the clock signal.

TCS The TCS input determines the number system interpretataion of the data input samples on pins DINO-7 as follows:
TCS = LOW — unsigned arithmetic
TCS = HIGH — 2's complement arithmetic

$\overline{\text{DIENB}}$ A low on this input enables the data sample input bus (DIN ∅–7) to all the MAC cells. A rising edge of the CLK signal occurring while $\overline{\text{DIENB}}$ is low will load the X REGISTER of every MAC cell with the 8-bit value present on DIN ∅–7. A high on this input forces all the bits of the data sample input bus to zero; a rising CLK edge when $\overline{\text{DIENB}}$ is high will load the X REGISTER of every MAC cell with all zeros. This signal is delayed by one clock internal to the chip. Therefore it must be low during the clock cycle immediately preceding presentation of the desired data on the DIN ∅–7 inputs. Detailed operation is shown on later timing diagrams.

CIN ∅–7 These 8 inputs are used to input the 8-bit coefficients. The coefficient is synchronously loaded into the Y REGISTER of MAC CELLO if a rising edge of CLK occurs while $\overline{\text{CIENB}}$ is low. The $\overline{\text{CIENB}}$ signal is delayed by one clock as discussed below.

TCCI The TCCI input determines the number system interpretation of the coefficient inputs on pins CIN ∅–7 as follows:
TCCI = LOW — unsigned arithmetic
TCCI = HIGH — 2's complement arithmetic

$\overline{\text{CIENB}}$ A low on this input enables the Y REGISTER of every MAC cell and the D registers (decimation) of every MAC cell according to the state of the DCMO-1 inputs. A rising edge of the CLK signal occuring while $\overline{\text{CIENB}}$ is low will load the Y REGISTER and appropriate D registers with the coefficient data present at their inputs. This provides the mechanism for shifting the coefficients from cell to cell through the chip. A high on this input freezes the contents of the Y REGISTER and the D REGISTERS, ignoring the CLK signal. This signal is delayed by one clock internal to the chip. Therefore it must be low during the clock cycle immediately preceding presentation of the desired coefficient on the CINO-7 inputs. Detailed operation is shown in later timing diagrams.

COUT ∅–7 These 8 three-state outputs are used to output the 8-bit coefficients from MAC CELL3. These outputs are enabled by the $\overline{\text{COENB}}$ signal. These outputs may be tied to the CIN ∅–7 inputs of the same DFP to recirculate the coefficients, or they may be tied to the CIN ∅–7 inputs of another DFP to cascade DFP's for longer filter lengths.

TCCO The TCCO three-state output determines the number system representation of the coefficients output on COUTO-7. It tracks the TCCI signal to this same DFP chip. It should be tied to the TCCI input of the next DFP in a cascade of DFP's for increased filter lengths.

$\overline{\text{COENB}}$ A low on the $\overline{\text{COENB}}$ input enables the COUT ∅–7 outputs and the TCCO output. A high on this input places all these outputs in their high impedance state.

DCM ∅–1 These two inputs determine the use of the internal decimation registers as follows:

DCM 1	DCM ∅	Decimation Function
∅	∅	Decimation registers not used
∅	1	One decimation register is used
1	∅	Two decimation registers are used
1	1	Three decimation registers are used

The coefficients pass from cell to cell at a rate determined by the number of decimation registers used. When no decimation registers used, coefficients move from cell to cell on each clock. When one decimation register is used, coefficients move from cell to cell on every other clock, etc. These signals are delayed by one clock internal to the chip.

SUM ∅–25 These 26 three-state outputs are used to output the results of the internal MAC computations. Individual MAC results or the result of the shift-end-add output stage can be output. If an individual MAC result is to be output, the ADRO-1 signals select the MAC result. The SHADD signal determines whether the selected MAC result or the output stage adder result is output. The signals $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ enable the most significant and least significant bits of the SUM ∅–25 result respectively. Both $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ may be enabled simultaneously if the system has a 26-bit or larger bus. However individual enables are provided to facilitate use with 16-bit bus.

$\overline{\text{SENBH}}$ A low on this input enables result bits SUM 16–25. A high on this input places these bits in their high impedance state.

$\overline{\text{SENBL}}$ A low on this input enables result bits SUMO-15. A high on this input places these bits in their high impedance state.